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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/789,352	02/26/2004	Yoko Sato	60538 (48229)	9123

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EXAMINER

RICHARDS, N DREW

ART UNIT	PAPER NUMBER
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2815

DATE MAILED: 06/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/789,352

Applicant(s)

SATO, YOKO

Examiner

N. Drew Richards

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 March 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10, 20 and 21 is/are pending in the application.
- 4a) Of the above claim(s) 21 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10 and 20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of group I, device claims 1-10, in the reply filed on 11/4/05 is acknowledged. Claim 21, as currently amended, is directed towards the non-elected method of group II and is no longer a linking claim. Thus, claim 21 is now withdrawn from consideration. Claim 21 defines a method that is patentably distinct from the claimed device since the claimed device could be made by a method different than that of claim 21. For example, the device as claimed could be made by a process including forming the first trench insulating layer and the second trench insulating layer in separate steps (not simultaneously).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-4, 7, 8 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by JP-2001-351995 (cited by applicant).

With regard to claim 1, JP-2001-351995 discloses in figures 36 and 37, for example, a semiconductor device comprising:

- a support substrate 2;
- an insulating layer 3 formed on the support substrate;

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- a first semiconductor layer 4 (left third of figure 36 and portion 42a of figure 37) formed on the insulating layer;
- a first high breakdown voltage transistor formed in the first semiconductor layer (either of the two transistors shown in the left third of figure 36 in high voltage region 42a);
- a second semiconductor layer 4 (left third of figure 36 and portion 42b of figure 37) formed on the insulating layer;
- a second high breakdown voltage transistor formed in the second semiconductor layer (either of the two transistors shown in the left third of figure 36 in high voltage region 42b);
- a first isolation region 45/47 formed between the first semiconductor layer and the second semiconductor layer, the first isolation region surrounding the first and second high breakdown voltage transistors and having a depth that reaches the insulating layer (as seen in figure 37, the isolation region 45/47 completely surrounds the different transistor regions 42a and 42b and is formed between the first and second semiconductor layers to the claimed depth);
- a third semiconductor layer 4 (middle third of figure 36 and any one of portions 44a-44f in figure 37) formed on the insulating layer;
- a first low breakdown voltage transistor formed in the third semiconductor layer;
- a second low breakdown voltage transistor formed in the third semiconductor layer; and

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- a second isolation region 5 formed in the third semiconductor layer between the first low breakdown voltage transistor and the second low breakdown voltage transistor, the second isolation region having a depth that does not reach the insulating layer.

With regard to claim 2, JP-2001-351995 further discloses a third isolation region 45/47 formed between the second semiconductor layer and the third semiconductor layer, the third isolation region having a depth that reaches the insulating layer.

With regard to claims 3 and 4, the first, second and third semiconductor layer are all of equal thickness.

With regard to claims 7 and 8, the surfaces of the first, second and third semiconductor layers are at a same level.

With regard to claim 20, this claim is merely broader in scope than claim 1 and thus JP-2001-351995 discloses all the limitations therein.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP-2001-351995, with evidence provided by Ning et al. (US 2004/0079993 A1).

JP-2001-351995 teaches the first, second and third semiconductor layers having the same thickness but is silent as to the thickness being 500 to 2000 nm. However, Official Notice is taken that it was well known to the skilled artisan at the time of the invention to form the semiconductor layers (SOI layers) to the claimed thickness. It is known to form the semiconductor layers to an large enough thickness to allow for proper device operation while keeping the layer thin to save on material and processing costs. These claims are prima facie obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range. In re Woodruff, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang, 40 USPQ2d 1685, 1688(Fed. Cir. 1996)(claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also In re Boesch, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and In re Aller, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious). As evidence that it is well known to form SOI semiconductor layers to the claimed thickness, see Ning et al. paragraph [0019] which teaches that typical thicknesses for the top silicon layer in an SOI are from about 5 to about 2000 nm. Thus, Ning et al. provides evidence in support of the Examiner's statement of Official Notice.

6. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP-2001-351995 as applied to claims 1-4, 7, 8, 20 and 21 above, and further in view of Kojima (US 5,965,921).

JP-2001-351995 teaches the first and second high breakdown voltage transistors comprising a first gate insulating layer 6 formed above a channel region, but does not teach a second gate insulating layer formed above an offset region and thicker than the first gate insulating layer.

Kojima teach high voltage MOSFET's in figure 1. Kojima teach a first gate insulating layer 3E formed above a channel region and a second gate insulating layer (unlabeled, thick insulator above 3C) above an offset region 3C wherein the second gate insulating layer is thicker than the first gate insulating layer.

JP-2001-351995 and Kojima are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to one of ordinary skill in the art to form the first and second high breakdown voltage transistors of JP-2001-351995 with the first and second gate insulating layers as taught by Kojima. The motivation for doing so is to improve the short channel effect or to reduce the gate drain capacitance and gate-drain breakdown. Therefore, it would have been obvious to combine JP-2001-351995 with Kojima to obtain the invention of claims 9 and 10.

Response to Arguments

7. Applicant's arguments filed 3/28/06 have been fully considered but they are not persuasive.

Applicant has argued that Shigenobu et al. do not disclose a first isolation region that surrounds the first and second high breakdown voltage transistors and has a depth that reaches the insulating layer. Applicant argues that the high-voltage transistors which adjoin mutually, are separated by the isolation layer 5, which does not reach the insulating layer. This argument is not persuasive. The "first" and "second" high voltage transistor of Shigenobu et al. are formed in separate transistor sections 42a and 42b (or alternatively in 42a and 42c, or 42a and 42d, or 42b and 42c, or 42b and 42d, or 42c and 42d) as seen in figure 37. These transistor sections (and the transistors therein) are separated from the other sections (and the other transistors therein) by isolation layer 45/47. Isolation layer 45/47 meets the claim language in that it has a depth that reaches the insulating layer 3. Thus Shigenobu et al. does disclose the claimed invention. It is noted that the language of the claims do not preclude the presence of more than one transistor in any of the claimed first or second semiconductor layers.

With regard to claims 5 and 6, Applicant timely traversed the Examiner's statement of Official Notice by requesting evidence by supplied. In response, the examiner has provided an evidentiary reference in the statement of the rejection above. This reference shows that it was known to form the silicon layer in an SOI structure to the claimed thickness. Thus, the rejection of claims 5 and 6 is maintained.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

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§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).


A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on Monday-Friday 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



N. DREW RICHARDS
PRIMARY EXAMINER